

LR-SoC: A Lightweight RISC-V SoC

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Low power consumption of edge processors for IoT is very crucial [1]. Therefore, designing a lightweight edge processor for IoT has drawn much attention lately [2]. In this paper, we propose a compact RISC-V SoC called LR-SoC. Fig.1 shows the architecture of LR-SoC. The core processor is an RV32IM processor which includes a barrel shifter and a debug module. The SPI controller is added to access flash memory. The 64KB of the on-chip memory (instruction cache) was chosen to make the fabricated chip compact yet effective. The boot memory contains 8KB of hard-wired code. The 8KB hard-wired code initializes the Control/Status registers (CSRs) in the RV32 core and displays the initial text on a monitor that is connected using the UART interface. The boot code loads the program from flash memory via the SPI interface and jumps to the on-chip memory where the loaded program is executed. With this booting flow, LR-SoC can self-boot to run any target application software from the SPI interface. The hardware implementation of LR-SoC was verified using Arty A7-35T FPGA. Synopsys tools were used for synthesis, and the implementation was synthesized using a Samsung 28nm process. The power consumption of LR-SoC estimated by Synopsys Power Compiler was 7.67mW. The performance of LR-SoC was evaluated by running the Dhrystone and Coremark tests. The results were 1.25 DMIPS/MHz and 2.94 Coremark/MHz, respectively. The silicon area of the core die is 0.015mm² and the measured operating frequency was 156MHz. Cortex A5, Rocket, and PULPv2 show 1.25, 1.38, and 1.02 times better performance than LR-SoC. However, they require a lot of silicon area and power consumption. Compared to the previous works, **LR-SoC shows 166 times smaller area and 16 times better power efficiency.** (이 내용이 맞나요?? 166 times more area 로 되어 있어서..)

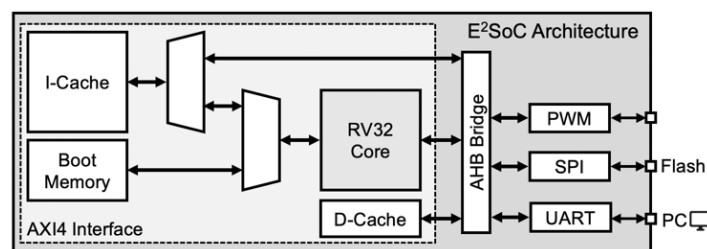


Fig. 1. Overview of E2SoC architecture

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References [1] E. Flamand et al., "GAP-8: A RISC-V SoC for AI at the Edge of the IoT." International Conference on Application-specific Systems, Architectures and Processors (ASAP), pp. 1-4. IEEE, 2018. [2] A. Garofalo et al., "PULP-NN: A Computing Library for Quantized Neural Network inference at the edge on RISC-V Based Parallel Ultra Low Power Clusters," 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 33-36. IEEE, 2019.